AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (canceled)

2. **(currently amended)** The semiconductor chip package as claimed in claim [[1]] 7, wherein

the interconnection substrate has a bottom surface provided with a plurality of contact pads around the recessed cavity;

the central substrate has a top surface provided with a plurality of first and second contact pads, wherein the second contact pads are electrically connected to the first contact pads;

the peripheral substrate has a top surface provided with a plurality of contact pads;

the semiconductor chip is provided with a plurality of bonding pads and disposed on the top surface of the central substrate by flip-chip bonding such that the bonding pads of the semiconductor chip are electrically connected to the first contact pads of the central substrate;

the central solder balls are electrically connected to the bonding pads of the semiconductor chip through the first contact pads of the central substrate; and

the peripheral solder balls are electrically connected to the semiconductor chip through the contact pads of the peripheral substrate and the second contact pads of the central substrate.

3. **(currently amended)** The semiconductor chip package as claimed in claim [[1]] 7, wherein the interconnection substrate comprises a top plate and a dielectric layer securely attached to the top plate, and the dielectric layer has an opening integrated with the top plate to form the recessed cavity of the interconnection substrate.

4. (original) The semiconductor chip package as claimed in claim 3, wherein the top plate of the interconnection substrate comprises a heat-sink.

5. **(currently amended)** The semiconductor chip package as claimed in claim [[1]] 7, further comprising a metal plate sandwiched between the semiconductor chip and the interconnection substrate.

6. **(currently amended)** The semiconductor chip package as claimed in claim [[1]] 7, wherein the central substrate and the peripheral substrate are mechanically and electrically connected to the interconnection substrate by a plurality of solder balls.

7. **(currently amended)** A semiconductor chip package, comprising:

an interconnection substrate;

a peripheral substrate having an opening;

a central substrate being disposed in the opening of the peripheral substrate and substantially coplanar with the peripheral substrate, wherein the central substrate and the peripheral substrate are mechanically and electrically connected to the interconnection substrate;

a semiconductor chip sandwiched between the interconnection substrate and the central substrate, the interconnection substrate having a recessed cavity for receiving the semiconductor chip;

a plurality of central solder balls disposed on a bottom surface of the central substrate and electrically connected to the semiconductor chip; and

a plurality of peripheral solder balls disposed on a bottom surface of the peripheral substrate and electrically connected to the semiconductor chip through the interconnection substrate;

wherein

the peripheral substrate is substantially separated from the central substrate thereby decreasing the stresses on the peripheral substrate due to coefficient of thermal expansion

mismatch; and

~~The semiconductor chip package as claimed in claim 1, wherein~~ the central substrate and the peripheral substrate are completely separated from each other.

8-27. (canceled)